sub E3

164. (Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value, wherein the binary value is representative of control information; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

Q1

165. (Amended) The method of claim 164 wherein the control information is representative of a number of clock cycles of an external clock signal to transpire before the memory device outputs data in response to a second operation code.

Q2

173. (Twice Amended) A synchronous memory device including an array of memory cells, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value that is representative of control information, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

174. (Amended) The memory device of claim 173 wherein the control information is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data and wherein the memory device outputs data in response to a second operation code.

183. (Amended) The method of claim 164 wherein the first operation code is issued to the memory device via an external bus.

Kindly **ADD** the following claims:

193. (New) The method of claim 164 wherein the control information includes a device type identifier.

194. (New) The method of claim 164 wherein the control information identifies a location of a defective portion of the array of memory cells.

195. (New) The method of claim 164 wherein the control information identifies a range of addressable locations of the array of memory cells.

196. (New) The method of claim 164 wherein the control information includes a device identification value to identify the memory device uniquely among a plurality of memory devices.

197. (New) The memory device of claim 173 wherein the control information includes a device identifier.

198. (New) The memory device of claim 173 wherein the control information identifies a location of a defective portion of the array of memory cells.

199. (New) The memory device of claim 173 wherein the control information identifies a range of addressable locations of the array of memory cells.

200. (New) The memory device of claim 173 wherein the control information includes a device identification value to identify the memory device uniquely among a plurality of memory devices.

201. (New) The memory device of claim 173 further including a plurality of registers, wherein the programmable register is included in the plurality of registers, and wherein the plurality of registers further includes at least one of:

a first register to store a value that identifies the memory device uniquely among a plurality of memory devices;

a second register to store a value that identifies a range of addressable locations of the array of memory cells; and

a third register to store a value that identifies a location of a defective portion of the array of memory cells.